REDUCED LEAKAGE CURRENT USING DOMINO TECHNIQUES

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ABSTRACT

As the aspect ratio of the devices shrinks down, the power supply voltage should be reduced to meet low power requirements, and the threshold voltage should also be reduced to achieve high performance. This, however, leads to exponential increase in leakage current; hence the circuit's reliability is also affected. A new domino circuit is proposed with reduced power and lower leakage for wide fan-in gates. The main goal was to make domino circuits more robust and with lower leakage and without dramatic speed degradation. The technique utilized in this paper is that, the pull-up network's mirrored current is compared with its worst case leakage current and it decreases the upper and lower boundary of the voltage swing on the dynamic node. The Dynamic node's parasitic capacitance and the keeper size for very high fan-in gates are also reduced by the proposed circuit. To implement fast and robust circuits the proposed circuit can be used as a small keeper for wide fan-in gates. The footer transistor is also used to reduce the leakage current. Simulation results of wide fan-in gates are designed using Tanner in 16-nm technology

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I. INTRODUCTION

DYNAMIC gates are used for implementing wide high-speed OR and AND gates in CMOS. These gates are especially used in multiport memories for low-power consumption[6]. Domino circuits are used for implementing high fan-in circuits and are widely used in high-speed applications [9]. With technology scaling, the supply voltage is reduced to decrease the power consumption and the threshold voltage is also reduced to achieve high performance. However, the threshold voltage scaling results in substantial increase of the subthreshold leakage current.

Hence the leakage current [11] must be reduced to obtain robust and high performance designs, especially for wide fan-in dynamic gates [15] which has many applications in digital signal processors and high performance critical units of microprocessors. However, in wide fan-in AND gate, with increasing leakage current, the robustness and performance significantly degrades. As a result, it is difficult to obtain satisfactory robustness and performance tradeoffs. In this paper, a Current Comparison based Domino (CCD) [8] circuit for wide fan-in applications is used which simultaneously increases the performance and decreases the power consumption.

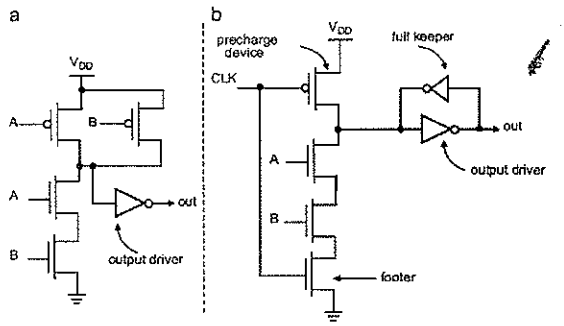

Figure 1 : Implementation of an AND gate in (a) CMOS and (b) nMOS domino Logic

Fig.1 shows the implementation of an AND gate using both static CMOS and NMOS domino logic [7]. In this circuit, to improve the robustness of the dynamic nodes a full keeper is added. The keeper ratio is defined as

$$K = \frac{\mu_p \left(\frac{W}{L}\right) Keeper - transistor}{\mu_n \left(\frac{W}{L}\right) evaluation - network} \quad (1)$$

where L and W denote the transistor size, and μ_n *and* μ_p are the electron and hole mobilities, respectively.

The robustness of domino circuits can be improved by varying the size (increasing) of the keeper transistor. However, this leads to the increase in delay of the circuit, power consumption, degradation of performance and also increase in the contention current between evaluation network and keeper transistor. As a large number of leaky nMOS transistors are connected to the dynamic node in wide fan-in dynamic gates the above mentioned problems becomes more critical.

Hence, there is a tradeoff between robustness and performance. Several circuit techniques have been proposed in the literature to address these issues such as a Standard Domino logic circuit with a Keeper (SDK) [14] (Power consumption is reduced using Low Swing Domino logic technique without reducing noise immunity), Low Swing Domino Circuit [10] (In this paper a LSD technique is used to reduce the power consumption and the voltage swing of a domino logic circuit and the noise immunity is improved), Two Input AND Gate with low inputs [13] (By operating the footerless domino circuits in idle and non-idle mode the gate oxide and subthreshold leakage currents are reduced).

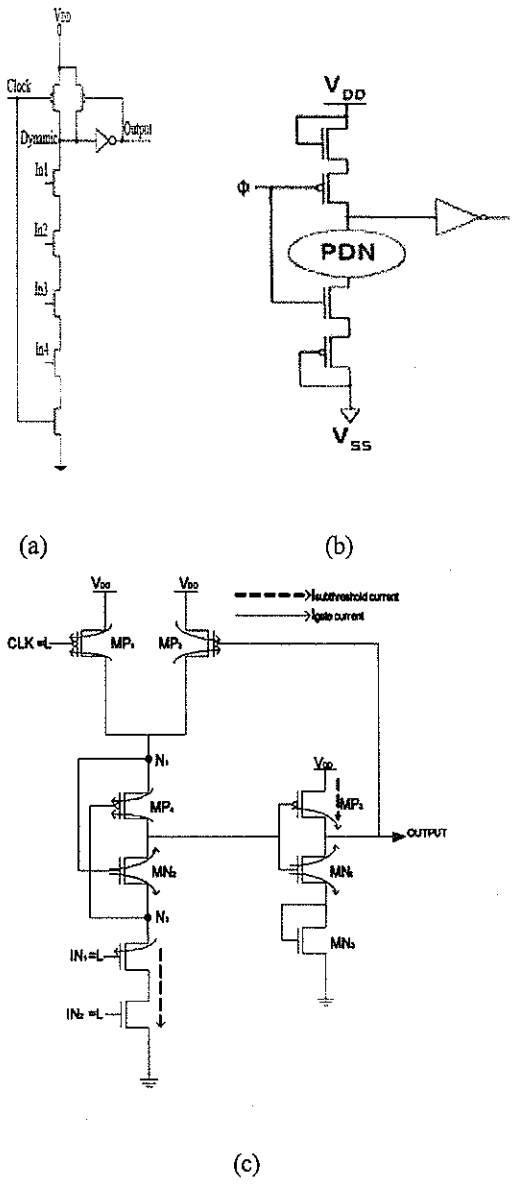

Figure 2 : (a) Standard Domino Logic Circuit with a Keeper (SDK), (b) Low Swing Domino Circuit, (c) Two input AND gate with Low inputs.

II. Proposed Circuit

In wide fan-in gates the dynamic node's capacitance is large. So, the speed is decreased dramatically. Varying the size (increasing) of the keeper transistor results in increased power consumption and delay that is due to increase in contention current. By using the comparison stage [8] the above problems can be solved by making the PDN to implement the logical function and separating it from the keeper transistor. In this stage, pull-up network's current is compared with its worst case leakage current.

This concept is illustrated in Fig. 3, where the PUN is used instead of PDN. However, there is a match between the reference current and the PUN. When the output node's voltage is dropped to ground voltage, the transistor M_K and the reference current are added in series to reduce power consumption.

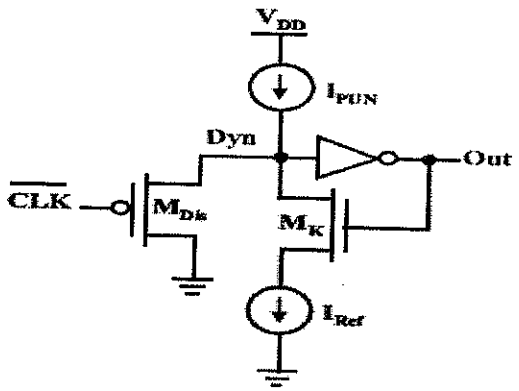

Figure 3 : Current Comparison Domino (CCD)

In order to maintain the robustness of the circuit, the reference voltage must be generated according to the correct variation of the reference current and process variations [1]. Process variations occur mainly due to systematic parameter fluctuations and random parameter fluctuations [2]. In random variations, the parameters of each device vary individually and it is independent of adjacent devices. However, in systematic variations the parameters of neighborhood transistors are affected, which leads to a strong correlation between parameters of nearby devices [3]. Systematic variations are considered in this paper. We have assumed that the threshold voltage of all nMOS and pMOS transistors varies together in a given circuit design. The speed of the circuit and power consumption [12] is directly affected due to any threshold variations on the voltage at node A and B. Hence these effects are carefully considered in the proposed circuit.

The worst case is that the threshold voltage of the pMOS is increased and the threshold voltage of the nMOS transistor is decreased i.e. due to process variations [4] it is slow pMOS and fast nMOS. In the former case, the pMOS transistor's subthreshold leakage in PUN is decreased; hence the reference current must be reduced and same for the latter case also. Therefore, in order to maintain the robustness of the design the reference current must be adjusted according to the variations in the threshold voltage.

The proposed circuit is shown in Fig. 4. The circuit in Fig. 4 is a replica of the PUN's worst case leakage current and correctly tracked leakage current variations that is due to process variations. Therefore, the transistor M_7's gate is connected to V_{DD}. As shown in Fig. 4, in the proposed circuit, transistor M_2 is used to mirror the current of the PUN with the reference current, which resembles the leakage current of the PUN.

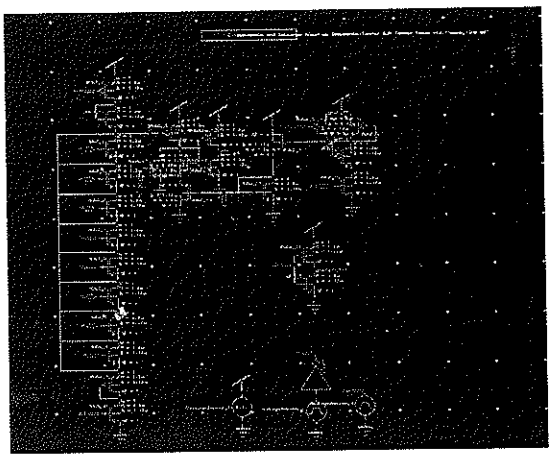

Figure 4 : Implementation of wide AND gate (8-input)

In the proposed circuit, nMOS transistors are used to implement the logic function, as shown in Fig. 4. The source and body terminals of the nMOS transistors are connected together in order to eliminate the body effect. So, the threshold voltage of the transistors is only varied and not the body effect due to process variations. By utilizing nMOs transistors in N-well process, the threshold voltage is reduced due to body effect, yielding a decrease in delay.

In other words, nMOS transistors can be used in P-well process to obtain a high speed due to higher mobility of nMOS. Although, the pMOS has lower mobility which reduces the speed, by reducing the capacitance on the dynamic node, the speed can be increased in the proposed circuit by properly choosing the mirror ratio M.

The proposed circuit as shown in Fig. 4 has five additional transistors and a reference circuit that is shared when compared to Leakage Current Replica Keeper (LCR) [5]. The transistor M_7's drain-source voltage is equal to the drain-source voltage of the pMOS transistors in PUN and all have the same V_{DS}. The transistor M_3's gate leakage is negligible when compared to the mirrored subthreshold current of the transistor M_7.

The proposed circuit operates in two stages. Preevaluation network is the first stage which includes the transistors , M_{Pre}, M_{Eval} and the PUN. The PUN, which implements the logic function, is separated from the dynamic node (DYN), which changes the dynamic voltage indirectly. The second stage resemble like a footless domino which has one input (i.e. node A input as in Fig. 4) that has no charge sharing with the transistor M_2 in spite of the Boolean function implemented by the PUN, and a controlled keeper that contains two transistors. To reduce the capacitance on the dynamic node, a pull-up transistor is connected to the DYN (dynamic node), yielding increase in speed. The first stage prepares the input signal for the second stage.

In the evaluation phase, there are two parts in dynamic power consumption, each for each stage. The dynamic power consumption is directly related to the voltage swing, capacitance, power supply, contention current and temperature. The first stage has no contention current and a low voltage swing from V_{SS} to V_{THP}. There is a rail-to-rail voltage swing at the second stage with minimum contention.

The proposed circuit has less dynamic power consumption even though it has some area overhead. In the proposed circuit, nMOS and pMOS transistors are used below the PUN and PDN respectively [10], to reduce and increase the upper and lower boundary of the voltage fluctuatuion at the dynamic node.

If the input to the AND gate is low, and if there is at least one conductive path exists between ground and node A, the voltage drop is raised up, which turns on the transistor M_2 and the output voltage is also changed.

Due to the unequal voltage of the body and source terminals, the body effect is not eliminated. If there is a higher deviation that is due to process variation the leakage current will be decreased further.

In the predischarge mode, the dynamic node is charged to power supply voltage that was at nonzero voltage at the starting. It results in the reduction of power consumption even when the dynamic node's capacitance is large in wide fan-in gates particularly for wide fan-in AND gates. Increasing the size of the transistor M_2 in turn increases the speed.

The mirror ratio M_2 is defined as the ratio of the size of transistor to the size of transistor M_1.

$$M = \frac{\left(\frac{W}{L}\right) M_2}{\left(\frac{W}{L}\right) M_1} \qquad (2)$$

The proposed circuit as shown in Fig. 4 operates in two phases as follows.

A. Predischarge Phase

In this phase, the clock voltage is at low level and the input signals are at high level [clk ="0", clk_bar ="1" as in Fig. 4]. The transistor M_{Dis} causes the voltages at the node A and the dynamic node to fall to a low level and its raised to a high level by transistor M_{Pre}. Hence the transistors M_2 and M_{Eval} are off and the transistors M_{Pre}, M_{Dis}, M_{k1}, and M_{k2} are on. The output inverter causes the output voltage to raise to a high level.

B.Evaluation Phase

In this phase, the input signals are at low level and the clock voltage is at high level level [clk ="1", clk_bar ="0" as in Fig. 4]. Hence the transistors M_2, M_{k2}, **and** M_{Eval} are on and the transistors M_{Pre} **and** M_{Dis} are off. Depending upon the input voltages the transistor M_{k1} can be on or off. Two stages occurs in this phase. All the inputs may remain high in first stage. Second, all the inputs may remain at the low level. At the first stage, the transistor M_2 mirrors the leakage current, which is compensated by the keeper transistors (M_{k1}, **and** M_{k2}) at the second stage.

The voltage at node A is decreased to nonzero voltage and the pull-up current is raised, when there is at least one conductive path exists in the second stage. The Mirrored current in transistor M_2 is raised by increasing the pull-up current. Hence the dynamic node's voltage is charged to Vdd. The voltage at the output node is discharged and the main keeper transistor M_{k1} is turned off. The simulated waveforms of the proposed circuit for 8-input AND gate is shown in Fig. 5. The results are obtained using 16-nm technology in TANNER software.

III. Simulation Results and Comparisons

The proposed circuit is designed using 16-nm technology in TANNER. 0.8V is used as the supply voltage and the wide fan-in (8, 16, 32, 64 input) AND gate circuit is used as a benchmark. The clock frequency used is 1-Ghz. The output capacitance load is set as 5 fF heavy load due to the high fan-out. Fig. 5 shows the simulations result of an 8-input AND gate using the proposed circuit

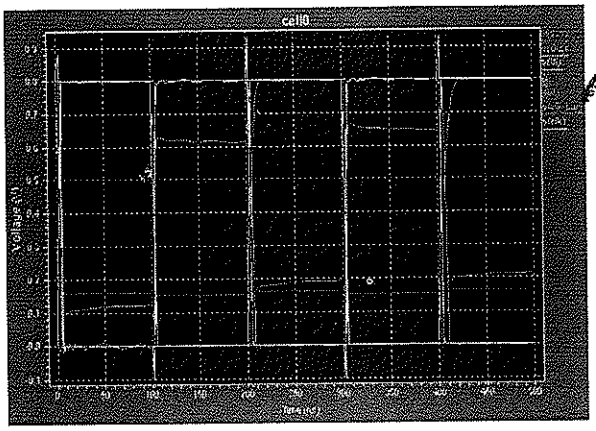

Figure 5 : Simulated waveforms of 8-input AND gate using the proposed circuit.

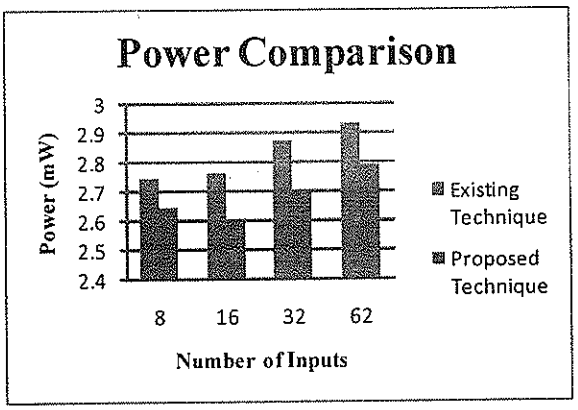

Figure 6 : Power comparison Results

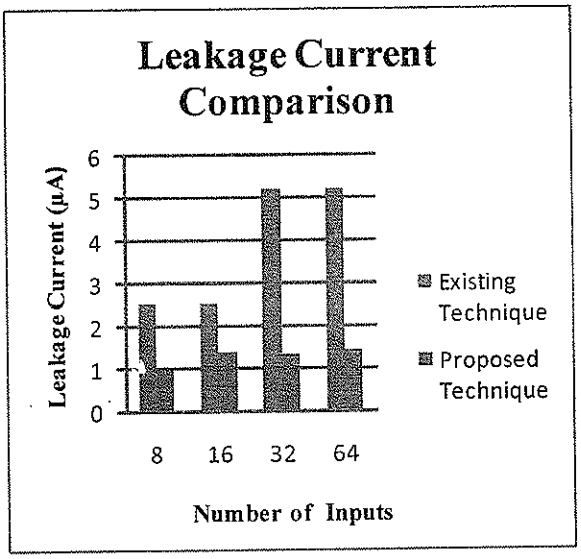

Figure 7 : Leakage current comparison Results

When all the inputs are at high level, the proposed circuit has lower leakage and it meets the high robustness required for wide fan-in gates. The overall leakage current of the proposed circuit is reduced to the source voltage of the PUN transistors. Fig .6 and Fig .7 shows that the power and the Leakage current is reduced in the proposed circuit. Subthreshold current is the major factor of the leakage current and is given by,

$$I_{Sub\_th} = I_0\left(1 - e^{\frac{-V_{DS}}{V_t}}\right)e^{\left(\frac{V_{GS}-V_{TH}+\eta V_{DS}}{nV_t}\right)} \quad (3)$$

with

$$I_0 = \mu_0 C_{OX}\frac{W}{t}(n-1)V_t^2 \quad (4)$$

where V_{GS} is the transistor gate-source voltage, V_{DS} is the transistor drain-source voltage, V_{TH} is the threshold voltage, $V_t = kT/q$ is the thermal voltage, η is the DIBL coefficient, n is the subthreshold swing coefficient of the transistor, μ_0 is the zero bias mobility, C_{OX} is the gate oxide capacitance, W and L are the width and length of the transistor. In the evaluation phase of the proposed circuit, when all the inputs are at high level, due to the leakage current the voltage at node A is decreased. The PUN transistors V_{SG} will be negative, and according to the above equations we get a lower subthreshold leakage current.

IV. Conclusion

With the technology scaling, the leakage current is increased dramatically in wide fan-in gates, resulting in increased power consumption and reduced noise immunity. The worst-case delay can be decreased by increasing the fan-in gates, which

in turn reduces the contention current between the evaluation network and keeper transistor. Simulation results show that the proposed circuit has lower leakage and reduced power consumption.

Thus, the proposed circuit can be used for implementing Boolean Logic functions for wide fan-in gates with reduced power and lower leakage.

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