Design of Bio-Medical Opamp

M. Santhana Lakshmi[1], B. Sudha[2] and P. T. Vanathi[3]

ABSTRACT

An operational amplifier for bio-medical application is proposed. The opamp includes rail-to-rail input stage, folded cascade stage with class AB biasing and a constant Gm stage. The opamp is made programmable to operate in two modes as low power mode and low noise mode. The opamp is realized in 130nm CMOS technology using H-Spice in Synopsis tool. The performed simulation shows a dc open loop gain of 97.755dB, CMRR of 112.41dB under a 22kÙ and 13.5pF load.

Index Terms Bio-Medical, low noise, low power, Operational amplifier.

1. INTRODUCTION

Currently, there is an ever-growing demand for low-power and low-noise mixed signal integrated circuits for applications such as portable medical systems. The operational amplifier (op amp) is the most important building block for analog signal processing. It is an active element with high-gain ratio designed to be used with other circuit elements to perform a specified signal-processing operation. The opamp is widely used for many applications; specifically opamp is mainly used in biomedical applications since the biopotential signals are of very low voltage that has to be amplified to certain level to process those signals. The opamp is used in biomedical applications like ECG and EEG, are impeded in a single chip. Design of the chip concern with low cost product and low noise behaviour but chip consumes high power. The opamp is developed with low noise, low power and low cost behaviour and it is made programmable by varying bias current given to it. The weak cortical biopotential input signals amplified with high gain.

The design of proposed opamp based on a circuit topology from [1] has been described. The opamp [2, 3] is implemented in 0.35μm CMOS technology using a supply voltage of 3.3V which has more power consumption and increased area. An application of the Opamp is described in [4] where it is used in the analog frontend (AFE) of a SoC for biomedical signal acquisition. The programming ability is exploited to set the AFE for optimal biomedical signal acquisition, e.g. low-noise mode for sensitive electroencephalogram (EEG) recordings or low-power mode for mobile electrocardiogram (ECG) applications. A 1.2V op amp has been integrated in a 0.35μm CMOS process [5] uses floating-gate input transistors in order to increase the input common mode voltage range of the opamp. The input common mode range of an op amp can

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be increased with the floating-gate transistors but due to the capacitive division the input signal is attenuated which results in deterioration of gain, GBW and noise properties. Opamp design is based on dynamic threshold voltage (DTMOS) transistors for low voltage bio medical applications (1V), low power and low noise applications [6]. The opamp is used to build the front-end receiver part of a near infrared spectroreflectometry (NIRS) device. The body and the gate are biased at the same potential in DTMOS transistors. The opamp is capable of processing ultra low-amplitude light signals. On the other hand, the the opamp circuits has more flicker noise (*1/f*), and makes it very harmful in this low-frequency bio medical applications because of its power spectrum and voltage offset.

2. BIOMEDICAL SYSTEMS

An integrated circuit has been widely used where ECG and EEG applications are impeded in a single chip. The most commonly observed biopotentials used in medical diagnoses can be monitored non-invasively with electrodes placed on the surface of the skin.These include the electrocardiogram or ECG which monitors heart activity; the electromyogram (EMG) which monitors other muscle activity in the body; and the electroencephalolgram (EEG) which monitors electrical activity in the brain via weak potentials on the scalp. This makes the chip unsuitable for mobile applications.Instead the integrated chip now widely where ECG and EEG applications are impeded in it.

The chip offers a relatively low-cost product for both ECG and EEG signals. The drawback is a high power consumption ensuring low noise behaviour for EEG applications. To overcome this problem, programmable components with adjustable trade-off between noise and power dissipation are most advantageous. These allow in

constructing a mobile ECG or EEG. Since the main noise source in the recording chain of biomedical signals is found in the first component, i.e. the preamplifier which consists of operational amplifiers, a programmable opamp is a key component.
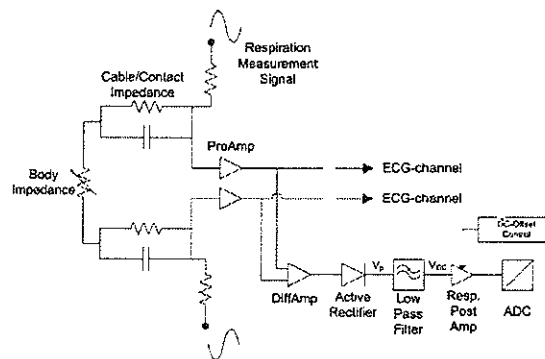
Figure 1. Bio-Medical System

The respiration monitoring system which is shown in the Figure 1 is fully integrated on chip with the exception of an external capacitor for low-pass filtering. The measurement principle is based on bioelectric impedance measurement on the patient's thorax and allows the measurement of respiration concurrently with an ECG-measurement using two ECG-electrodes. The circuit is also used to detect open-leads by measuring the absolute impedance between leads. If this impedance exceeds a certain threshold, the leads are assumed to be open. The on-chip oscillator generates two differential 40 kHz sine-signals, which are applied to the body-electrodes through additional impedances forming a voltage divider. The applied carrier-signal is modulated by a change of body impedance due to breathing of the patient.

After the preamplifiers, both the ECG-signal and the modulated carrier are present., because the carrier is located at 40 kHz, which is removed by the low-pass filter at the end of the analog channel, respiration measurement does not disturb ECG measurement. After the

preamplifiers, the differential carrier is converted to a single-ended signal. The very-low-frequency (<1 Hz) respiration signal modulated on the carrier signal can be considered as a slow varying DC-signal. To extract this DC-signal an active full-wave rectifier is used followed by a Sallen-Key low pass filter. The obtained respiration signal is too small (in the microvolt range) to be directly A/D converted. Therefore, an adjustable post amplifier is used to amplify this signal. The amplified respiration signal is finally AD converted and the digitized signal can be read out by the on-chip DSP.

3. EXISTING OPAMP ARCHITECTURE

A. Introduction

In this section, opamp architecture is described. The opamp architecture in [7] has improvements over gain, power and noise performance. The objective of the work is to use the most promising programmable low-power and low-noise opamp. Eventhough the opamp described here provides considerable increase in gain, reduction in noise and power, the proposed opamp architecture has shown more improvement in parameters such as gain, CMRR, slew rate and reduction in noise.
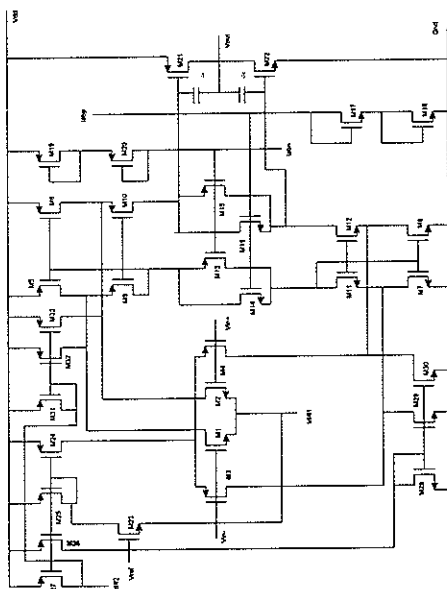

Figure 2 : Existing Opamp Architecture

In biomedical applications, opamp needed to be developed which consumes less power, offers less noise and need to amplify the weak cortical input signals to a larger extent. This opamp is able to work within a programming range being in low-noise mode at one end of the programming range and in low-power mode at the other. An application of the Opamp is that used in the analog front end (AFE) of a SoC for biomedical signal acquisition.

From Figure 2, the transistors M1-M4 form a rail-to-rail input stage, M5-M20 a folded cascade stage with class-AB biasing for the output stage M21 and M22. The constant-gm stage is formed with transistors M23, M25-M33 to enable the programmability. The remaining transistors used for distribution of bias currents and generation of bias voltages. Programmability is controlled by external bias currents Idiff1,2 and Iabn,p, the external voltage Vref sets the switching point of the constant-gm stage. Voltages Vbcn and Vbcp are used for biasing of the cascode stage and capacitors Cc for Miller compensation.

B. Opamp Design Using Low Supply Voltage

The folded-cascode stage with transistors biased in strong inversion is set to two constraints for the minimum supply voltage branch of the cascode:

$$V_{dd} \geq 5 * V_{ov} \tag{1}$$

$$V_{dd} \geq 2 * V_{gs} + V_{ov} \tag{2}$$

with the overdrive voltage Vov = Vgs - Vth. The Equation2 can be rearranged with respect to the maximum threshold voltage Vth,max into

$$Vth, max \leq \frac{1}{2} * (Vdd - 3 * Vov) \tag{3}$$

If an overdrive voltage of Vov = 0.2 V for strong inversion is taken, then Equation1 leads to a minimum supply voltage of Vdd = 1 V. A supply voltage of Vdd = 1.2 V satisfies Equation 1. Then Equation 3 is satisfied only when the threshold voltage is less or equal than 300 mV.

The transistors with the lowest threshold voltage values of Vthn = 0.38 V and Vthp = -0.33 V for minimum channel length can be taken. However, if channel lengths of the lowest threshold voltages and if it is 5 or more times larger than minimum length, the threshold voltages reduce to a value of Vthn ~ Vthp ~ 0.25 V because of reverse short channel effects (RSCE) [8]. Using these transistors with the appropriate channel length, opamp works properly.

A. Programmability Of Opamp

To keep the phase margin constant over the whole programming range, a constant ratio of the input and output transistors transconductance is needed [9]. And hence the ratio transconductance of the output stage Gm22 to the transconductance of the input stage Gm4 is maintained constant as indicated in the Equation 4. The input stage transistors are biased in weak inversion and the folded-cascode and output stage transistors are biased in strong inversion

$$\frac{Gm22}{Gm4} = \frac{\sqrt{Id22}}{Id4} = const \tag{4}$$

The ratio of cascode stage current I_{D12} to output stage current I_{D22} is also kept constant and hence to $I_{D4}{}^2$ sinks via M30 before it reaches the cascode stage. This is also done for I_{D3} by transistor M29, and the same current sinking is performed by M32 and M33 for the NMOS input pair. The bias currents for the input stage are set by the external currents Idiff1 and Idiff2. Here the external bias current values for the input stage are taken as 286µA for high power and low noise mode. The bias currents for the folded cascode and output stage are set by the external currents Iabn and Iabp. Here the external bias current values for the folded cascade stage and output stage are

taken as 30µA for high power and low noise mode. Simulation and measurement done with |Idiff1| = |Idiff2| and |Iabn|= |Iabp|. Three distinct modes of operation for opamp as low-power (Plow), medium-power (Pmedium) and high-power (Phigh).

B. Proposed Opamp Architecture

In biomedical measurements the common mode rejection ratio (CMRR) is an important parameter indicating the ability to reject the power line interference [10]. Two important limitations for the CMRR are to be considered when using active electrodes. One is the potential divider effect. Any difference in the skin-electrode impedance will limit the maximal CMRR where stands for the impedance of the amplifier. The CMRR of the biomedical amplifier is given as

$$CMRR \approx 20 \log \frac{2\Delta Z_{el}}{Z_{in}+2Z_{el}} \tag{5}$$

ΔZ_{el} be the difference in the skin-electrode impedance and Z_{in} be the input impedance of the amplifier. Gain is also an important parameter which can also be improved by increasing the output resistance of the amplifier. In bio medical opamp ,the input noise of both electrodes is mainly the input noise of a MOS transistor. The noise can be reduced by using the folded structures or by reducing the bias currents passing through the input stages. For a single MOS transistor the thermal noise density can be expressed as

$$e_n = \frac{4TK_B}{G_m} \cong \frac{4TK_B}{\sqrt{2\beta I_{bias}}} \tag{6}$$

Where K_B denotes the Boltzmann constant, T is the temperature, G_m is the transconductance and I_{bias} be current flow through the amplifiers input stage.
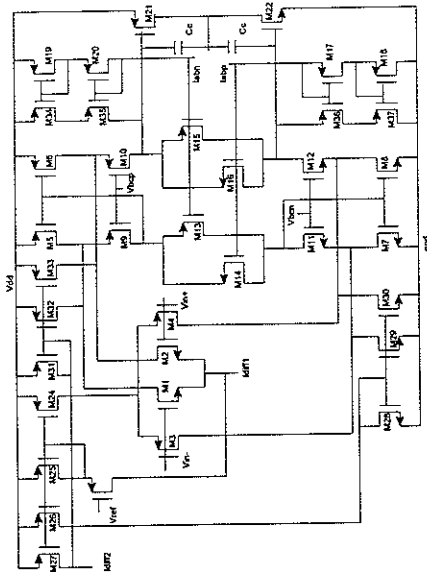
Figure 3. Proposed Opamp Architecture

The current mirror is one of the main building blocks of analog and mixed-signal integrated circuits. Current mirrors are used inorder to achieve high accuracy and high output impedance. Cascode stages are widely use in different circuits to boost gain in amplifiers or to obtain a higher precision on current mirrors, without adding new current-consuming stages.

From the existing biomedical opamp shown in Figure 2, the diode connected transistors M17, M18, M19, M20 at the output side are replaced with the cascode current mirrors formed by the transistors M17- M20 and M34-M37 in order to increase the CMRR and gain of the opamp. The proposed opamp includes both NMOS current mirror and PMOS current mirror. The proposed biomedical opamp shown in Figure 3 includes the both NMOS current mirror and PMOS current mirror at the output stage.

4. SIMULATION RESULTS

The opamp architectures were implemented using HSPICE in Synopsis tool and gain, power, noise, CMRR

and slew rate values were obtained. Figure 4 gives the gain plot of the proposed bio-medical opamp.
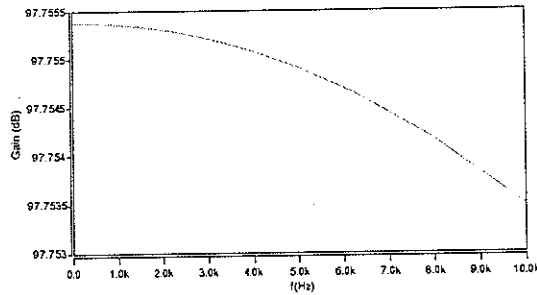

Figure 4. Gain plot of the proposed opamp

Settling time behavior is performed for the proposed opamp in Figure 3 with the voltage follower configuration. Figure 5 Shows the step input given to the non-inverting terminal of the proposed bio-medical opamp. The output is feedback to the inverting input terminal. Figure 6 shows the settling time output of the proposed bio-medical opamp.
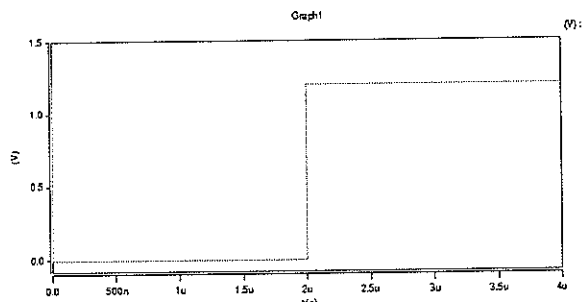

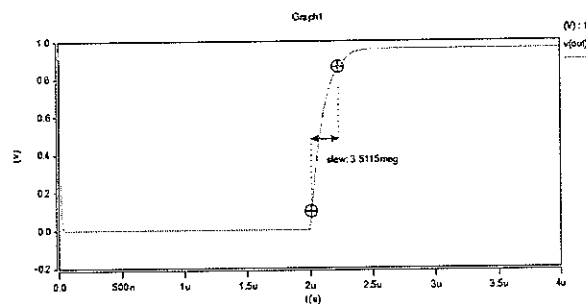**Figure 5. Step input to the proposed opamp**

Figure 6. Settling time output of the proposed opamp

AC analysis is performed for the proposed biomedical opamp in Figure 3 with the common mode configuration as shown in Figure 7.
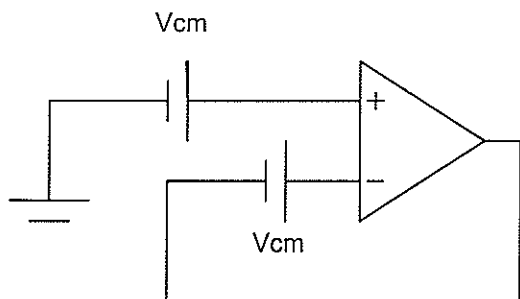

Figure 7. Common mode configuration of the opamp

The common mode configuration for calculating CMRR is simulated. Figure 8 shows the CMRR output of the proposed bio-medical opamp.
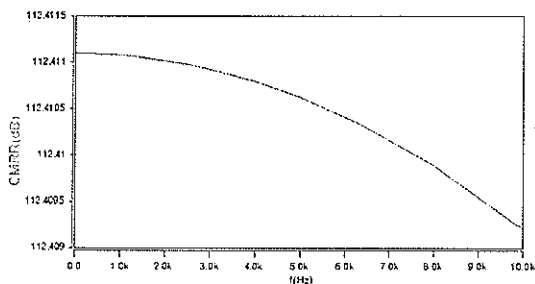

Figure 8. CMRR of the proposed opamp

The proposed bio-medical opamp circuit in the Figure 3 is simulated and the results are tabulated in Table 1. It is inferred from the table that, the proposed bio-medical opamp achieves improved performance in the parameters such as gain value of 97.7554dB , low noise of about 2.155 nV/$\sqrt{Hz}$ at 200KHz, CMRR of about 112.41dB, THD

of about -75.354dB and slew rate of about 3.5115V/μS under load of 22kΩ and 13.5pF.

PARAMETER	UNITS	EXIST -ING OPAMP	OPAMP with Cascade Current mirror
Power Dissipation	mW	0.719	0.73
Open Loop Gain	dB	95	97.7554
Unity Gain	MHz	9.7479	9.2
Frequency Total Harmonic Distortion (Input Voltage = 1Vpp,Freq= 1Khz,Gain=1)	dB	-75.352	-75.354
Input Thermal Noise (@ 200k)	nV/$\sqrt{Hz}$	4.84	2.155
Slew Rate	V/μS	0.13	3.5115
Supply voltage	V	1.2	1.2
CMRR	dB	105	112.41
Load conditions R_L C_L	Ω F	22k 13.5p	22k 13.5p

Table 1 Comparison of Existing and Proposed Architectures

5. CONCLUSION

A 130nm programmable CMOS operational amplifier has been proposed. The opamp developed consumes less power, offers less noise and it amplifies the weak cortical input signals to a larger extent. The proposed opamp shows the improvement in the gain of about 2.755dB, common mode rejection ratio of about 7.41dB , reduction in noise of about 2.685 nV/$\sqrt{Hz}$ and increase in slew rate of about 3.3815 V/μS compared to that of the existing opamp. So the proposed opamp can take part in the biomedical applications like ECG,EEG,EMG in which the device need to be compact for low power and low noise applications.

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