FPGA Applications in DC - AC Converters : A Single Chip Implementation of Spwm and SVPWM Modulators

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Abstract

In the past decade, the development in the field of FPGA has found a lot of applications in electrical power conversion applications. The SPWM and SVPWM are the most commonly used PWM schemes in the three phase inverters due to their advantages. This paper presents single chip implementation of two commonly used PWM schemes such as SPWM and SVPWM in a single FPGA using Q-format data representation. It also provides the guidelines and quick references for practicing engineers and researchers in the field of FPGA based development to select the suitable digital controller based on the switching frequency, speed of the algorithm and single chip applications.

Key words : FPGA, SPWM, SVPWM, Q- format, Single chip implementation, VHDL.

1. Introduction

For over 100 years, the three phase ac induction motor has proven to be an extremely reliable electromechanical conversion device. For the vast majority of that period, it evolved as a constant speed device operating from a constant frequency, constant voltage, and sinusoidal utility power source [1-2]. The power conversion and its future have been discussed in the literature [3]. Pulse Width Modulation (PWM) has been studied extensively during the past decades [4-5]. Many different PWM methods have been developed to achieve the better performance such as: wide linear modulation range; less switching loss; less total harmonic distortion (THD) in the spectrum of switching wave form; and easy implementation and less computation time [6-14][27-39].Many three-phase loads require a supply of variable voltage variable frequency (VVVF), with a fast and high-efficiency control by digital electronic means. The conversion of dc power to three-phase ac power is exclusively performed in the switched mode using proper switching by means of suitable PWM algorithm. The actual power flow in each motor phase is controlled by the on/off ratio, or duty-cycle of the respective switches. The desired sinusoidal waveform of the currents is achieved by varying the duty-cycles sinusoidally with time, employing the techniques of PWM. The schematic of PWM controlled three phase inverter is shown in Fig. 1.

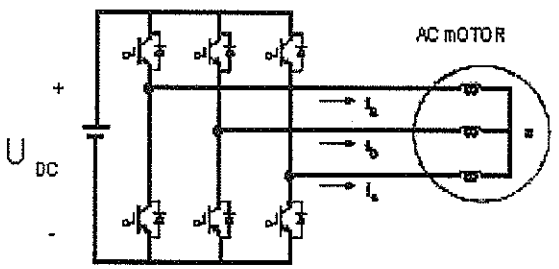

Figure 1 : Schematic of Three phase Voltage source inverter

The Space Vector Pulse Width Modulation (SVPWM) technique has been widely studied over the decades for power converter applications such as ac-dc converters,

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power factor correction, power system analysis and dc-ac inverters [27-28, 37-39]. In dc-ac converters, SVPWM gives a higher output voltage for the same dc-bus voltage, lower switching losses, and better harmonic performance in comparison with the carrier-based Sinusoidal Pulse Width Modulation (SPWM). Therefore, SVPWM scheme becomes the preferred PWM technique for various three-phase power converter applications used in ac drives, UPS and power conditioning equipment.

The unpredicted development in industrial drives and power conditioning equipment over the past decades is resulted from the process developments demanded by the automation industry. This is further augmented with increased speed of modern microprocessors, micro controllers, digital signal processors (DSP's), complex programmable logic devices (CPLD), application specific integrated circuit (ASIC) technology and Field programmable gate array (FPGA) based control techniques used in reduced insulated gate bipolar transistor (IGBT) drive package size, coupled with ac motors leads to achievement of multiple machine configuration with minimal process down time. Among all these possibilities, FPGA is a good compromise between the advantage of the flexibility of a programming solution and the efficiency of a specific architecture with a high integration density.

Digital technology has greatly impacted the design of controls for power electronics. In the beginning, when only low-performance processors were available, writing code for controllers was largely an art form, without a well-defined and standardized design procedure. With the advent of DSP's and high-performance processors in general, the design approach has significantly changed [9-14]. In the literatures DSP based control of PWM in power converters for the applications such as ac drives and power conversion [6-15] has become area of research due to its features of simple circuitry, software control and flexibility to adapt various applications.

FPGA has been extensively used for many industrial and control applications such as servo control, robotics, and multi-processor based control, monitoring system, power measurement systems, and power converter control [16-26]. Also in telecommunication industries FPGA has been used extensively. This paper elaborates the FPGA based PWM generation techniques for dc-ac converter used in ac drives.

Therefore, in past decades, motor control and power conversion ICs employing ASIC/FPGA technology are receiving more attention [15-48]. Traditional software-based systems suffer disadvantages of complex circuitry, limited functions, difficult circuit modification, high cost and low executive speed. In addition, the traditional design cycle is even longer than the life cycle of modern electronic products. But the great success of very large-scale integration (VLSI) technology has given us a perfect solution. In the literature, the recent power electronic control applications are implemented with FPGA –ASIC due to its reconfigurability. The emergence of FPGA and CPLD as well as top-down EDA methodology gives the designers a good chance to arbitrarily design their own ASICs in their labs, and not in the semiconductor factories, with only a personal computer and a download cable. FPGA is somewhat different from CPLD in inner structure, but their usage is basically the same.

In DSP-FPGA based control implementation, the arithmetic functions are carried out by the DSP processor [27, 37-39] and the PWM generation is carried out in FPGA. The draw back of the FPGAs is: it is difficult to implement the arithmetic functions, equations in the PWM algorithm and the signal processing technique

handled is integer representation which leads to error in the output. The drawbacks of the DSP-FPGA based control scheme are complexity in interfacing, system is bulky, long development time, and need of expertise in both technologies. Nowadays, an embedded control and IP design can be developed and downloaded into FPGA to construct a System on Programmable Chip (SoPC) environment for ac drive systems [23]. The details of IP core are given in [48,52]. The literature [49] gives details of floating point representation and the corresponding IEEE standard. Therefore it is advisable to use a single FPGA for the system to overcome the above difficulties using Q-format [50-51]. Using this format, it is possible to implement the arithmetic functions in the FPGA. The different data format and Q- format are discussed in the section-III.

This paper presents survey of FPGA applications in power electronic converters especially for dc-ac converters with single chip FPGA implementation. Also "The FPGA based VLSI Architecture for Single chip SPWM and SVPWM Modulator" has been implemented using a new methodology, Q –format for signal processing which enables the development of the entire SPWM and SVPWM on a single chip. The SPWM architecture has been designed and implemented using VHDL and FPGA. The literatures referred will gives the details of selection of the device, design procedures, switching frequency and so on.

The remaining paper is organized as: Section II- FPGAs and the development tools; Section III - Fixed point formats; Section IV - FPGA applications in power industry, implementation of PWM controls with simulation results; and Section V - Conclusion.

2. Description of FPGAs and their development tools

2.1 FPGA Description

FPGA belong to the wide family of programmable logic components. Their densities are now exceeding 10 million gates. FPGA can be defined as a matrix of configurable logic blocks (combinatorial and/or sequential), linked to each other by an interconnection network that is also entirely re-programmable. Memory cells control the logic blocks as well as the connections so that the component can fulfill the required application specifications. Several configurable technologies exist, but we are interested in FPGA among these re-programmable devices (Flash EPROM, SRAM), since they allow the same flexibility of a microprocessor. The generic architecture of this type of FPGA is as shown in Fig. 2.

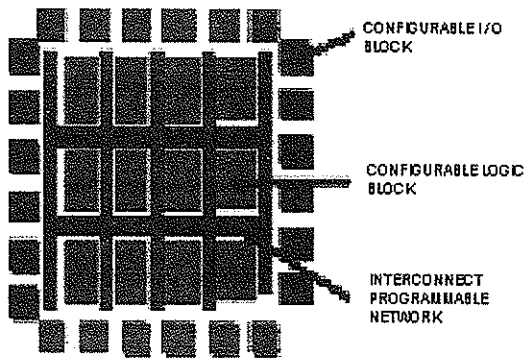

Figure 2 Generic Architecture of an FPGA

The architecture of the above FPGA is composed of a matrix of configurable logic blocks (CLB), which is bordered by a ring of configurable input/output blocks (IOB). Finally, all these resources communicate among themselves through a programmable interconnection network.

2.1.1. Hardware Description Languages and FPGA

Originally, FPGA were only used to replace basic logic circuits and their applications are described with the help

of simple CAD schematic tools. Today, FPGAs are more and more utilized to implement complex functions. For example, a complex system consists of an Arithmetic Logic Unit (ALU), motor control units, PID controllers, memories, communication units, and so on.

This evolution of FPGA is due to the development of appropriate design tools and methods, which took their origin from the VLSI circuit technology. These tools are mostly based on Hardware Description Languages (HDL) such as Very high-speed integrated circuit Hardware Description Language (VHDL) or Verilog.

The existence of an IEEE standard has spread the use of VHDL and has allowed the creation and the development of high performance CAD tools in the field of microelectronics. Thus, the designer can take advantage of this language to build his own circuit by using a hierarchical and modular approach that is defined at different levels of abstraction. Design approach by abstraction levels can be applied to ASIC as well as to FPGA and is referred in the literature as "top-down methodology".

The FPGA design flow is given as follows:

- *The system level*
- *The behavior level*
- *The Register Transfer Level (RTL)*

At each level of abstraction, the future integrated circuit is described in HDL such as behavior VHDL or synthesis VHDL. The last description gives an exact representation of the operators and variables of the final circuit. In order to simulate and validate the digital circuit functionality, various test benches are written and executed. The Fig. 3 shows the hierarchical flow of the top-down design method and its HDL model environment.

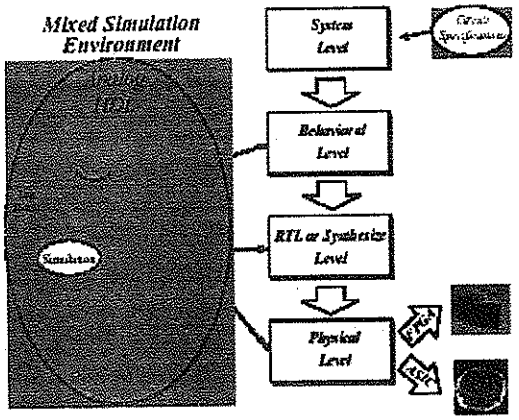

Figure 3 The Hierarchical flow of the top-down

Presently, FPGA manufacturers have designed software packages that both enable the simulation and the automatic translation into hardware design. This software runs inside the Matlab-Simulink environment and results are "bit and cycle accurate". It should be mentioned that the concept of automatic code generation has already been applied with success to DSP processors.

2.2 Design Methodology

FPGA technology allows the development of specific hardware architecture within a flexible programmable environment. This specificity of the FPGA gives the designer a new degree of freedom when compared to microprocessor implementations since the hardware architecture of the control system is not imposed a priority. However, in many cases, the development of this architecture is rather intuitive and not adapted to the implementation of more and more complex algorithms. Thus, in order to benefit from the advantages of the FPGA and their powerful CAD tools, the designer has to follow an efficient design methodology. Such a methodology rests on two main principles: the modularity and the best suitability between the algorithm to implement and the chosen hardware architecture.

2.3 Design Methodology based on reuse modules

For very complex designs, modular conception is generally used to reduce design cycle. This methodology is based on hierarchy and regularity concepts. Hierarchy is used to divide a large or complex design into sub-parts called modules that are more manageable. Regularity is aimed at maximizing the reuse of already designed modules. With the ceaseless increasing progress of CAD tools, the improvement in terms of development time reduction lies more on the designer to know how to classify and reuse his module models than a perfect knowledge of his CAD tools. Nowadays, the manufacturers and the designers of circuits even propose to recover in free or restricted access, several design models, also called Intellectual Property (IP) modules [48].

We understand that per module, an element of a library, available to the designer can be directly inferred without having to design it. Therefore, the reuse methodology consists of selecting throughout the synthesis process, the elements of a library that are useful for the design. These modules extracted from the design flow are distributed between the various levels of abstraction. The procedure of doing so is very similar to those used in DSP development with soft-macros.

3. Fixed point formats

Systems employing micro controllers, DSP's, and Programmable Logic Devices (PLDs), the technique commonly used for signal processing is integer fixed point approximation, except in the new generation floating point DSP's. The accuracy of the processed results depends on data approximation employed in arithmetic computations. Hence it is proposed to implement Q- format approximation in signal processing applications.

3.1 Types of data formats

There are two main types of formats commonly used for real time signal processing [49-50].They are: (i) Fixed point representation and (ii) Floating point representation.

Most of the digital systems use integer fixed point format due to area consideration. The main drawback of this Format is erroneous result. In most of the applications this erroneous result is within acceptable range and the error value depends on the processor used [27,37-39]. In case of FPGA based single chip controllers like the SVPWM controller, the algorithm is implemented without any other external controllers. Therefore in single chip applications, it is important to consider the error because it may lead to loss of accuracy.

The Q-format (Q-indicates "Quantity of Fractional bits") [50-51] technique is a compromise between integer formats and floating point formats. One of the main advantages of SVPWM is less harmonic distortion in the output of inverter. Therefore while processing harmonic related data using integer fixed point format, the harmonic analysis is inefficient, because the resultant data contains considerable amount of error. This work mainly concentrates the implementation of PWM in a single FPGA using Q-format.

If the application demands mainly accuracy, less computational overhead, less area, etc then the best choice would be binary form of 2's complement representation. This is the only method to represent the negative numbers by means of binary format. Hence, it is necessary to improve the accuracy of the binary form of representation for real world data and it can be met using Q-format. The Q-format is an efficient technique when compared to integer format for fractional numbers as and when the design concentrates on accuracy.

3.2. Real data representation in Q - format

The IEEE -754 standard [49] describes the floating point representation for signal processing with 16 bit and 32 bit formats. A QN format number is an N bit 2's complement binary number; a sign bit followed by an N bit mantissa (fraction). QN format can be used to express numbers in the range -1 to $(1 - 2^{-N})$.

Q Format Notation [50-51]

The position of the binary point in a fixed-point number determines how to interpret the scaling of the number. When it performs basic arithmetic such as addition or subtraction, hardware uses the same logic circuits regardless of the value of the scale factor. In essence, the logic circuits have no knowledge of a binary point. They perform signed or unsigned integer arithmetic. The position of the binary point in the signed, fixed-point data types is expressed and designated by Q format notation. This fixed-point notation is represented in the form

Qm.n

where, Q designates that the number is in Q format notation, the Texas Instruments representation for signed fixed-point numbers.

m is the number of bits used to designate the two's complement integer portion of the number.

n is the number of bits used to designate the two's complement fractional portion of the number, or the number of bits to the right of the binary point.

In Q format, the most significant bit is always designated as the sign bit. Representing a signed fixed-point data type in Q format always requires m+n+1 bits to account for the sign.

a. Example: -Q.15

For example, a signed 16-bit number with n = 15 bits to the right of the binary point is expressed as Q0.15

In this notation, (1 sign bit) + (m = 0 integer bits) + (n = 15 fractional bits) = 16 bits in the data type. In Q format notation, the m = 0 is often implied, as inQ.15

b. Example: -Q1.30

Multiplying two Q.15 numbers yields a product that is a signed 32-bit data type with n = 30 bits to the right of the binary point. One bit is the designated sign bit, thereby forcing m to be 1: m+n+1 = 1+30+1 = 32 bits. Therefore, this number is expressed as Q1.30

c. Example: - Q2.17

Consider a signed 16-bit number with a scaling of 2(-17). This requires n = 17 bits to the right of the binary point, meaning that the most significant bit is a sign-extended bit. Sign extension fills additional bits with the value of the MSB. For example, consider a 4-bit two's complement number 1011. When this number is extended to 7 bits with sign extension, the number becomes 1111101 and the value of the number remains the same. One bit is the designated sign bit, forcing m to be -2: m+n+1 = -2+17+1 = 16 bits total. Therefore, this number is expressed as Q - 2.17.

d. Example: -Q17.-2

Consider a signed 16-bit number with a scaling of 2^(2) or 4. This means that the binary point is implied to be 2 bits to the right of the 16 bits, or that there are n = -2 bits to the right of the binary point. One bit must be the sign bit, thereby forcing m to be 17: m+n+1 = 17+(-2)+1 = 16

Therefore, this number is expressed as Q17.-2

An XQN format number is a QN format number left shifted by X bits. XQN format can be used to express numbers in the range: (-2X) to (2X - $2^{(X-N)}$).The 1QN format representation is given in table-1.

Table 1. 1QN Data format

Range	Sign bit	D8	D7	D6	D5	D4	D3	D2	D1
+1	0	1	0	0	0	0	0	0	0
-1	1	1	0	0	0	0	0	0	0
+II / 4	0	0	1	1	0	0	1	0	0
-II / 4	1	1	0	0	1	1	0	1	1
		^ ← Binary point							

3.3. Analysis of representing real-world data in integer and Q-format

The error in the signal processing depends on the type of data format used for representing signal. The theoretical analysis for the operation of addition is carried using different formats.

3.3.1. Analysis Example

For Example real data: 0.2625

a. Representation: Integer Format:

The Integer representation using truncation for fractional part is INT [0.2625*2^7] = INT [33.6] = 33 = 00100001

The Integer representation using rounding for fractional truncation is INT [0.2625*2^7+0.5] =INT [34.1] =34= 00100010

b. Representation: 1Q8 Format:

+0.2625=0001000011

c. Addition operation: Integer Format:

34(00100010) + 34(00100010)=68(01000100)

The resultant data will be ($68/2^7$)=0.53125. The actual result should be 0.525.

d. Addition in Q8 Format:

0.2625(001000011)+0.2625(001000011)=0.525(010000110)

The resultant data will be 0.525. In this format the result obtained is equal to the actual value of 0.525.

When comparing the results for addition in integer and Q- formats, it is observed that the error in integer format is 0.625% where as in Q format error is zero.

Generally in digital circuits, multiplication is performed by repeated addition. Therefore multiplication in integer format will also have error which depends on the binary bits and number of additions. The table -2 shows the error in the output of the different types of data formats for 8, 16 and 32 bit representation.

Table 2. The error in the output of the different types of data formats

Type of data representation	% error(for 8 bit representation)	% error(for16bit representation)	% error(for32bit representation)
Fixed point integer Format by rounding method	0.625	0.002	-0.000000009
Q-format	0	0	0

From the analysis, Q-format will give more accurate result as compared to traditional integer formats and is the best method for developing the entire process in a single FPGA. Even though integer format gives less error which leads to inferior performance, it is not suitable for the dynamic range of -1 to +1 and also processing in a single FPGA

4. FPGA IN APPLICATIONS POWER INDUSTRY

FPGA has been employed in electrical power conversion applications such as dc-dc converters, power supply control, dc-ac converters, ac-ac converters, power factor

correction, power measurement systems, monitoring systems and also in telecommunication industries.

4.1. Applications of FPGA in three phase inverters

In the last decade, the FPGA has been used in the power converters to generate the PWM pulses with a microprocessor interface commonly DSP. The Integer fixed point type of data representation and processing is used in FPGA implementations[27,37-40]. In order to improve accuracy the new generations of floating point DSPs are used in ac drives.

4.2. Implementation of SPWM and SVPWM

The most commonly used PWM schemes are SPWM and SVPWM, therefore the single chip FPGA implementation of these schemes are implemented and analyzed for the feasibility in power converter applications

4.2.1. Implementation of SPWM

The designed VLSI Architecture for SPWM modulator is shown in Fig.4. The internal modules of the SPWM architecture are Q –format arithmetic logic unit (QALU), clock divider, frequency selector, CORDIC core [52], PWM Controller and dead time module. In FPGA implementation the QALU is constructed as generic library functions.

Each module is described with VHDL and compiled and simulated in the environment of Xilinx. In [27,36-39], the arithmetic functions in FPGA implementations has been carried out using integer approximations with additional auxilary controlers, usally DSPs. Due to single chip implementation the integer approximations fails to give accuracy in the dynamic range of -1 to +1, therefore Q-format representation is used to implement the SPWM modulator. In FPGA implementation the QALU is constructed as generic library functions. The QALU performs all arithmetic and logic functions in Q-format representation.

4.2.2. Results and Discussion

The SPWM modulator has been simulated using ModelSim-5.7g simulator. The SPWM waveforms with a switching frequency (fz) of 20 kHz and a fundamental (f_o) of 50 Hz are shown in Fig.5 and Fig. 6. In fig. 5. In fig. 5, the simulated three phase output voltage waveform is shown.

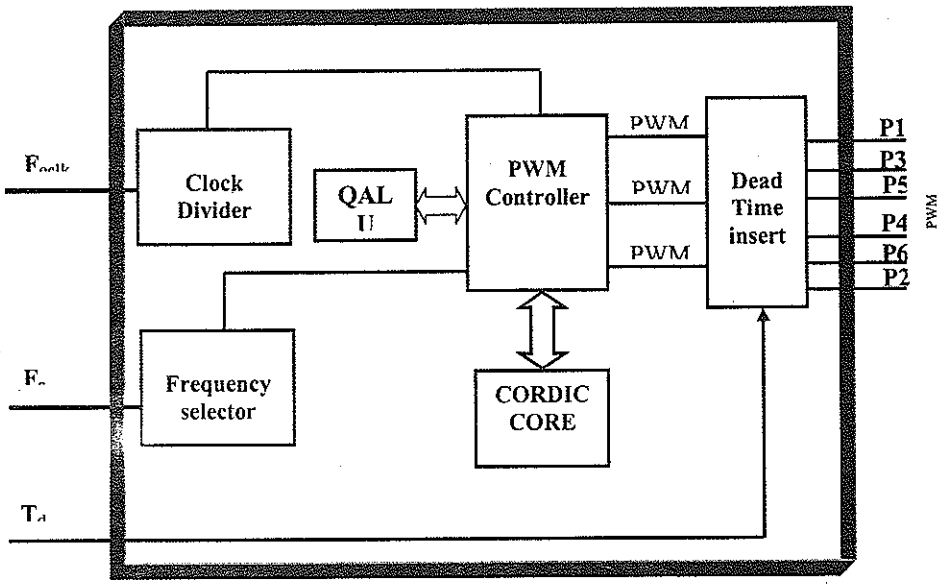

Figure 4 : The Proposed VLSI Architecture for SPWM

The fundamental as well as the switching frequency is programmable. The results shown below are the PWM pulses applied to the three phase dc-ac converter. The FPGA based single chip SPWM modulator can be used as modulator for high performance ac drives.

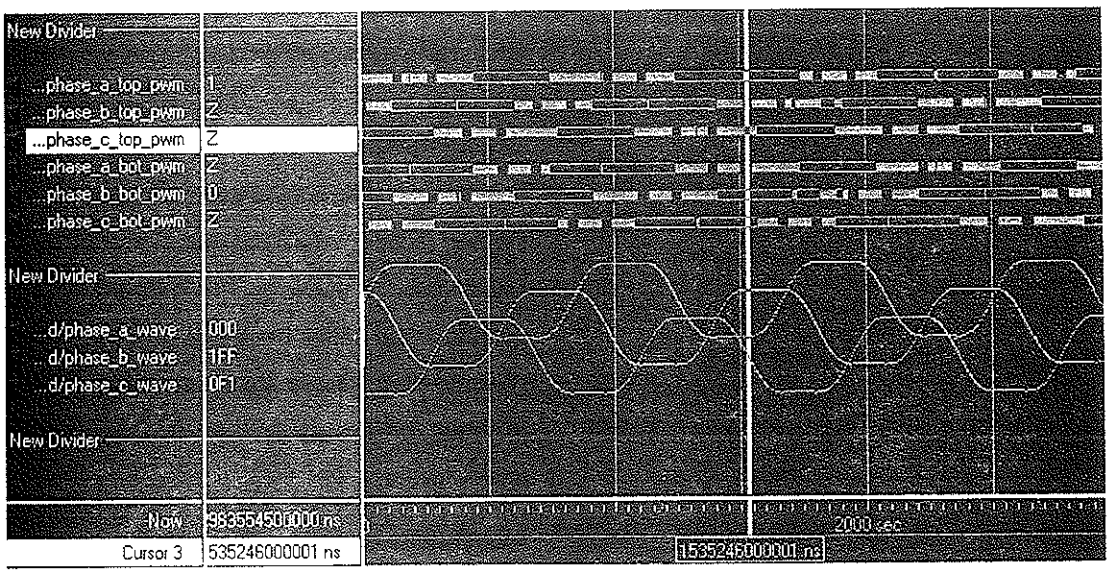

Figure 5 : PWM wave forms in three phases with Tz=2.63 kHz, f0 = 50 Hz

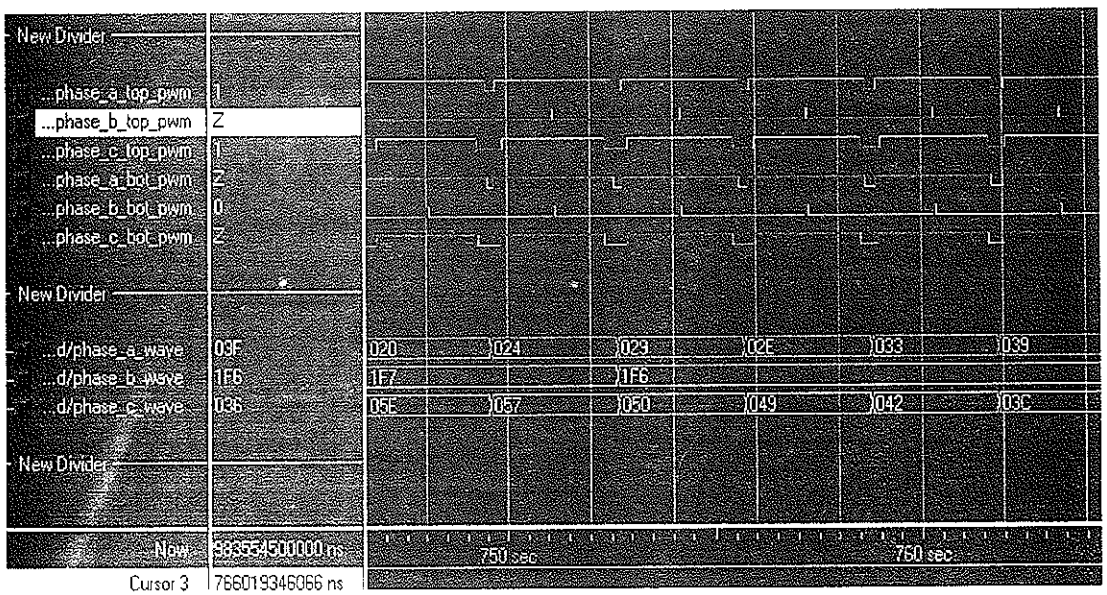

Figure 6: SVPWM output for f_s = 40 kHz and f = 50 Hz

4.3. Implementation of SVPWM

The SVPWM Architecture for single chip applications is shown in Fig. 7 is designed and implemented in FPGA. The internals of this Architecture consists of QALU, transformations, sector detection, PWM generator, delay time generator and sin/cos generator. The data and the

arithmetic operation handled are using Q –format. To carry out the arithmetic operations an ALU is designed called QALU. In FPGA implementation the QALU is constructed as generic library functions.

The basic requirements for realizing the SVPWM is to first receive the three phase voltage from the inverter instead of receiving reference vector and phase from external processor[37-39], and to compute the orthogonal components of the voltage vector. Second, these 2-axis orthogonal components are converted to 3-axis components, and then these three-phase PWM waveforms are converted to centralized encased PWM waveforms with minimal switching. Finally, the PWM gating signals are inserted with adjustable time delay to protect the phase legs from short-circuiting.

4.3.1. Simulation Results and Discussion

The SVPWM modulator has been simulated using ModelSim-5.7g simulator. The SVPWM patterns for all sectors have been achieved for different switching frequency with the fundamental of 50 Hz. The results for Fz = 6 kHz and 6 MHz are shown in Fig. 8 and Fig. 9 respectively. The fundamental as well as the switching frequency are programmable, based on the requirement. The results shown are the pulses applied to the three phase dc- ac converter for ac drives.

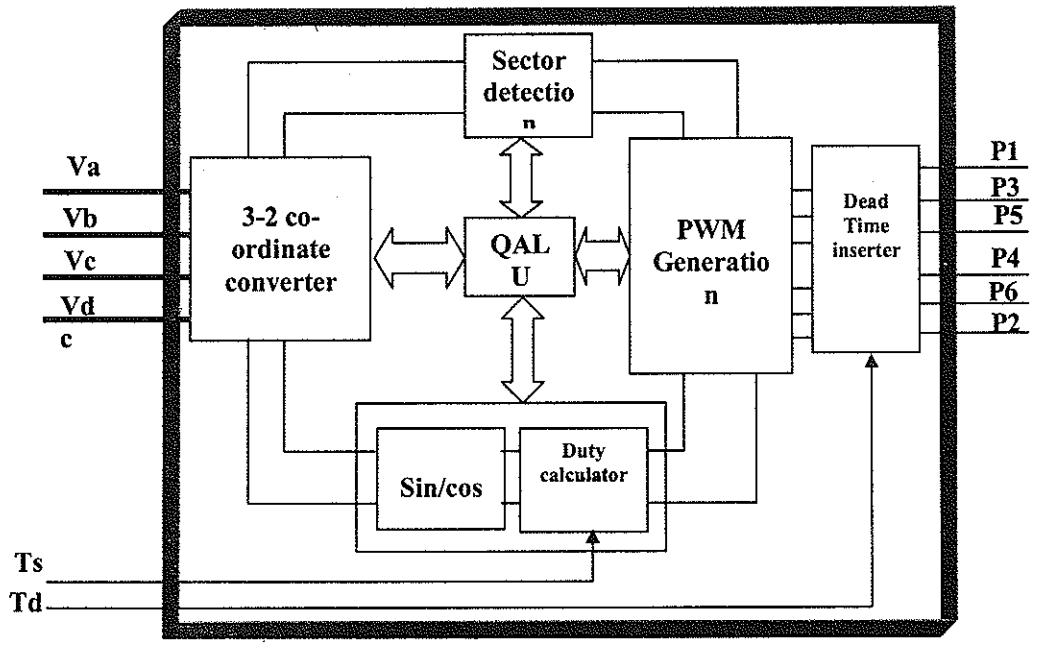

Figure 7 The Proposed VLSI Architecture for SVPWM

5. Conclusion

In this paper the FPGA based PWM generation for dc-ac converter used in ac drives are elaborated. The SPWM and SVPWM, the most commonly used PWM schemes, are implemented in a single FPGA using Q-format data representation. Also this paper presents the guidelines and quick reference for practicing engineers and researchers in the field of FPGA based digital controls. FPGAs can be used for many industrial, and control application such as servo control, robotics, multi-processor based control, monitoring system, power measurement systems, and power converter control in

addition to the major electrical power conversion applications.

6. ACKNOWLEDGEMENT

The authors would like to thank the Management of Karpagam College of Engineering (KCE) Coimbatore, TN. and Jawaharlal Nehru Technological University (JNTU), Hyderabad, AP., India for providing all infrastructural facilities during this work.

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